Open-Silicon Provides Complete Semiconductor Solutions from Concept to Production

Interview with Taher Madraswala
President and CEO of Open-Silicon

The DisplayPort Display Interface

Build an Arduino from Scratch
The LRDIMM Advantage

Prior to 8 Gb DRAMs, 32 GB LRDIMMs were constructed using more expensive DDP 1 packaged 4 Gb DRAMs, as shown in Figure 2. In 32 GB 4RX4 LRDIMMs based on 4 Gb DRAMs, two DRAM data loads from the frontside DDP and two from the backside DDP share the same data bus. These four DRAM data loads are further reduced down to one data buffer load by the LRDIMM’s unique data buffering architecture.

Figure 2

Because of this data load reduction technique, when populating three LRDIMMs in a memory channel, only three loads are present. In addition, the nine data buffers are physically located very close to the edge connector, reducing data transmission stub length. Reducing transmission stub lengths and stub counts improve signal integrity. Figure 3 shows a memory controller channel (MCH) configured with three LRDIMMs (3 DPC). Improving signal integrity adds more signal margin, thereby improving server system reliability when populating thousands of memory modules into thousands of servers at a typical data center.

Figure 3

1 DDP = Dual Die Package. 2 DRAM die in a single DRAM package

PRODUCT WATCH

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- AE Petsche Interconnect Products

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INDUSTRY INTERVIEW

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For this Arrow New Product Insights, we’ll highlight some of the features and benefits of Microchip’s PIC microcontrollers and dsPIC® digital signal controllers.

Microchip’s PIC MCU ecosystem is built to deliver the best user experience, accelerating development, enabling seamless transitions between platforms, and delivering innovative peripherals to enhance design capabilities.

The PIC microcontroller family allows developers to quickly scale designs up or down as the design evolves, requiring higher performance, lower power, or additional functions, saving the time and cost of designing in new hardware and recoding for new platforms. This is due to the common design ecosystem that covers the full 8- to 32-bit performance spectrum and protects the investment in code development. Scalability is further facilitated by the availability of pin-compatible, drop-in replacement hardware bridging product families. PIC MCUs and dsPIC DSCs also integrate innovative peripherals to implement complex functions, simplify development and reduce total solution footprint and cost.

To support development with all of its MCUs and DSCs, Microchip provides free award-winning tools as part of its NetBeans-based MPLAB® X IDE, MPLAB Code Configurator (MCC) and MPLAB Harmony Integrated Software Framework. MPLAB X IDE is also extensible via third-party plug-ins and software and integrates seamlessly with programmers, debuggers, simulators, and emulators. All of this is supported by free code libraries, webinars, application notes, and reference designs. This tight integration between a comprehensive hardware and software ecosystem helps developers deliver their products to market faster and at a lower cost.

PRODUCT FEATURES

- **MPLAB X IDE**
  - Supports all MCUs and DSCs
  - Free C compilers, software libraries
- **MPLAB Code Configurator (MCC)**
  - Graphical programming environment
  - Automatic peripheral/function configuration and code generation
- **MPLAB Harmony Integrated Software Framework (ISF)**
  - Code abstraction
  - Libraries, drivers, system services, middleware, third-party code
  - RTOS integration

Harmony Integrated Software Framework. MPLAB X IDE is also extensible via third-party plug-ins and software and integrates seamlessly with programmers, debuggers, simulators, and emulators. All of this is supported by free code libraries, webinars, application notes, and reference designs. This tight integration between a comprehensive hardware and software ecosystem helps developers deliver their products to market faster and at a lower cost.

KEY FEATURES

- 8-bit, 16-bit, 32-bit PIC MCUs
- 16-bit dsPIC® DSCs
- Flexible memory technologies
- Upward compatible architecture
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- Configurable Logic Cell
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INTERCONNECT PRODUCTS

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A.E. Petsche, a leader in interconnect components traditionally serving the aerospace and defense industry has expanded their reach into the rail industry. Today we are proud to present our TE connectivity Rail products; we will be focusing on 9 rail products including Wire and Cable, Connectors and Terminals, and Cable Identifiers.

**100E**

The 100E series of signal wire and cable from TE Connectivity is zero-halogen, small-size, and both flexible and non-wrinkling making it perfect for low voltage applications. The 100E meets approvals of EN50306-2, -3, and -4, and has a continuous operating wire temperature range from -55 Celsius to 125 Celsius. This cable is available from 1 to 4 conductors and has a voltage rating of 300 volts.

**100G**

The 100G series of signal wire and cable comes with a halogen-free polymer insulation rated at 750 volts. This cable is available with conductors ranging from 1 to 9 and with wire sizes ranging from 0.15 sqmm, using 19 strands of wire, down to 4.00 sqmm which uses 56 strands of wire. The high number of wire strands makes the wire very flexible. For single core cables the part number includes a designator for determining cable color in accordance with Mil Standard 681.

**400R**

TE’s 400R series of signal wire and cable is in the family of rail approved 600 volt wires and cables. This series of cable is available in cores of single, double, triple, and quad with an operating temperature range from -65 Celsius to 125 Celsius. And, while operating at 125 Celsius the cable’s life span is 10-years, but at 110 Celsius the life span is increased three-fold to 30-years. Conductor sizes range from 26 gauge down to triple-ought, and the outer jacket colors are available from codes 0 to 9 using Mil Standard 681.
In addition to rail cable and wiring, A.E. Petsche also offers high-speed data cables.

The line of AMPPOWER terminals, splices, and quick disconnects from TE are ideally suited for power generation and distribution in rail, mass transit, power transmission and military markets. Their reliable technology of mechanical compression crimping eliminates variables common to other crimping methods, such as melting temperatures, flux composition, entrapped gases, or oxidation. These connecting solutions are made from either high-quality seamless copper tubing or high-quality brass bar stock along with tin or silver plating which makes for high conductivity and corrosion protection.

TE’s M12 cable connectors include features of 360-degree EMI and RFI shielding along with torsion and vibration-proof cable strain relief. These connectors are available in 4, 5, or 8 poles, have a temperature rating of -20 Celsius to 85 Celsius, have operational voltage options of either 30VDC or 50VDC, and can transmit up to 10 giga-bits-per-second. The angled M12 cable connector 90-degree flex is especially suited for harsh conditions due to the crimp termination for both the signal contact and the cable shield. With data transmission rates up to 100 mega-bits-per-second this special design of 8 cable exit options provides the flexibility to solve any installation condition.

The CIRP series cylindrical connectors are based on the latest performance requirements of MIL-C-5015. These connectors represent proven electrical capability where durability is most important. Features include threaded couplings and single key polarization representing maximum simplicity in design. Typical applications include Rolling Stock, Sub Systems Equipment, infrastructure & signaling and Maintenance, Repair & Overhaul.

In addition to cables and connectors, A.E. Petsche also offers wire and cable identification sleeves. TE’s HX-SCE series are low-fire hazard heat shrinkable sleeves which are cut and organized into a ladder format. Typical applications include mass transit, rail, aerospace, marine and industrial.

The ZHD-SCE series of heat shrinkable sleeves are the next generation of cable identification solutions. They are unique in the sense that they are both low-fire-hazard AND diesel resistant. Until now heat shrink cable identifiers were either one or the other—but never both—which makes them the first and only heat shrink cable identifiers of their kind on the market today. They have a temperature range of -55 Celsius to 125 Celsius, sleeve diameters from 2.4mm to 38.1mm, and a shrink ratio of 2:1.

For more information on the latest TE Connectivity products offered through A.E. Petsche visit our website at aepetsche.com/te.
For this installment of TechXposed, we show how to build an Arduino from scratch. After downloading the Arduino Eagle files from Arduino's official site, we sent the boards to be manufactured and purchased all the required parts from onlinecomponents.com.

We recently acquired a low-priced Chinese laser cutter and used it and an overhead transparency to make a solder paste stencil. Using the cream layer from our Eagle file, we output an image we were then able to import into the software. We found that, by far, the best method was to fill in the holes in the image, instead of solely having an outline of the holes. From there, we set the program to engrave; not cut, which works fairly well for making the small holes.

Next, we line up the stencil and the board properly. Using some double-sided sticky tape, we tape the PCB onto a flat surface. Place the transparency over the board, carefully lining it up with the holes. Duct tape on all four corners holds the stencil firmly in place. Once everything is secure, paste can be applied. Using a simple...
Putty scraper, push the solder paste into the holes and give the solder paste a flat top.

Now we can place the parts of the Arduino. First, we'll place the reset button, which is tied to the reset pin on the microcontroller, the ICSP programmer, and the reset pin in the headers. There are two varistors on the board, attached to the two data lines of the USB, helping keep the lines clean from excess voltage without affecting the data signals. Between these two varistors is a 22-ohm resistor array put in series with the data signals to act as termination resistors. A PTC, or resettable fuse, is placed in series with the incoming power from the USB to trip if the board pulls too much current, protecting your computer’s USB.

Next is an Atmega 16U2 that acts as a USB to serial converter, which makes a place to simply hook a USB up to the board without worrying about an FTDI cable. The QFN is also one of the more difficult parts to solder, as the pads are tiny and a very precise balance is needed between enough solder paste to make the connection but not so much that it will bridge. The alignment, however, is relatively easy, as it self-adjusts during reflow to line up on the pads more exactly.

We then have a dual op-amp. One op-amp acts as a buffer for a voltage divider and controls the 3 point 3 volt LDO, and the second op-amp controls the communication status LED. There is also an LDO that accepts the 7 to 12 V input via the barrel jack and drops it down to 5V. This is directly followed by the LDO that drops the 5V down to 3.3V. The last surface mount device is a final diode to make sure that there isn’t any current flow back into the barrel jack.

We now very carefully put it into our cheap reflow oven which, other than the awful smell it produces, works rather well. Inside the oven, if you look closely, you can see the solder flowing and changing, becoming very shiny. You’ll also see the small passives moving a bit as they get sucked onto the pads better, though sometimes this results in tombstoning or other issues. The larger devices, such as the electrolytic capacitors, take more time to heat up and flow.

Now we’ll finish up with the through hole devices. For the first part of this step, we put on the 16 megahertz crystal that the USB to serial microcontroller uses. We then need to trim the leads before moving on. Next comes the the socket that the DIP package microcontroller sits in, followed by the headers. Finally, we drop the USB and the power connector on and the project is complete.

The time and effort to assemble a single board this way is non-trivial. However, it’s a great way to learn more in depth about the electronics that are out there and get some practice with prototyping assembly techniques.
Ohmite has researched, developed, and applied thick film technology for power and high voltage resistors for over fifty years. These applications require the ability to dissipate heat, and now Ohmite is taking that experience and knowledge and applying it to generating and directing heat. Many applications need more than just a heater, requiring heat to be applied evenly across a surface, or to apply heat in certain areas, but not others. Ohmite partners with customers to leverage their expertise in thermal analysis and design and the special printing techniques they’ve developed to direct heat precisely where the customer needs it.
Thick film heaters can be placed near uninsulated metal without a risk of shorting or arcing, have a small, low-profile footprint, and many different substrates can be used based on the application need. Ohmite has also developed the unique ability to produce traces with variable width, enabling very evenly distributed heat patterns.

Screen printing thick film heaters results in very predictable, uniform heat distribution, and can be done using a variety of substrate materials, shapes, and patterns while remaining cost competitive with previous technologies. Ohmite’s process supports variable trace thickness to easily create areas with different heating characteristics. Ohmite R&D engineers are continuously testing different combinations to provide customers with baselines to work from to meet the needs of different applications. Ohmite is also able to screen print NTC or PTC thermistors in the heater circuit to shutdown the heating element once a predetermined surface temperature has been reached.

Thick film heaters are able to address a wide range of applications due to their performance and flexibility, currently supporting voltages up to 240 VAC and power up to 1000 W. These include small, low-power devices such as security camera lens defoggers and personal hair products just as well larger and more demanding applications such as large food and beverage warmers, automotive battery warmers, or deposition chamber dryers.

For more on Ohmite thick film heaters or to start working on your next design, go to Ohmite.com.

Uninsulated Metal

Screen printing thick film heaters

Variable trace thickness

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Variable trace thickness
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When it debuted in May 2006, DisplayPort was ahead of its time and faced stiff competition from HDMI in high-definition consumer electronics devices. The latter had already carved out a niche, and went on to become a nearly ubiquitous interface across millions of TVs, monitors, desktop video cards, Blu-ray players, gaming consoles, and even laptops. DisplayPort, meanwhile, had only made its way into a few new PC monitors and digital signage displays. Fast-forward 10 years and we see a different situation: The rapid dissemination of 4K resolution monitors demands greater video bandwidth for maximum performance than that which can be supplied through contemporary HDMI. Achieving 4K resolution at anything beyond a 60-Hz refresh rate now requires DisplayPort. Worth noting, though, is that buying into the technology is a long-term investment, because DisplayPort allows for daisy-chaining multiple 4K displays, or future-proofing for 5K (5,120 x 2,880) and 8K (7,680 x 4,320) resolutions.
DisplayPort is a license-free, royalty-free video and audio interface standard that allows both internal and external display connections. The standard was developed by the graphic processing unit (GPU) and display industry and is administered by the Video Electronics Standards Association (VESA). It was designed to replace the analog-VGA (video-graphics-array) and DVI (digital-visual-interface) interfaces in PCs, monitors, and eventually consumer electronics, as well as the internal board-to-display LVDS (low-voltage-differential-signaling) links in PCs and consumer electronics. DisplayPort features a high degree of interoperability by bridging multiple standards and device types.

Products that include DisplayPort
The number of products certified in DisplayPort is at an all-time high, and it is available as a display interface on a wide range of desktop GPUs, monitors, notebooks, tablets, and even television panels. This is different than the high-budget GPUs and monitors for which it was initially designed, but thanks to the increasing demand for 4K displays and smaller devices with flexibility connectivity, wider integration is only expected to rise. VESA saw the number of devices sold increase by 63% in 2013, and in 2014, this figure jumped to 73%—from 805 to 1,395 devices.

What’s more, Embedded DisplayPort (eDP) adoption is expected to grow in tandem with the embedded display market, which is expected to reach a combined $12.8 billion by 2020, with a compound annual growth rate of 12.44% (between 2014 and 2020) across multiple industries—automotive, construction equipment, medical, fitness equipment, wearables, home appliances, HVAC, and industrial automation.

THE BENEFITS OF DISPLAYPORT INCLUDE:

- **High-performing capability**
  Bearing in mind that DisplayPort is a much newer standard, and one that was initially designed as a PC-to-monitor interface for high-performing graphics displays, it makes sense that the format leverages updated signal and protocol technology. DisplayPort is also the first display interface to use packetized data transmission like that which is used in USB, PCI Express (PCIe), SATA, and Ethernet. It integrates the clock signal within the data stream and permits a single clock source to regulate as many output streams as can be supported by the GPU, thereby elevating the display interface from a mere pixel pipe to one that can transmit audio and video simultaneously.

With its high-bandwidth capabilities, DisplayPort supports very high resolutions, color depth, frame rates, and multiple displays without needing to compress the image data sent from a GPU. For example, DisplayPort 1.2 supports 4K (4,096 x 2,160) resolution at a 60-Hz refresh rate, while HDMI 1.4 can sustain only 4K at 24 Hz or 4K UHD (3,840 x 2,160) at 30 Hz. More recently, DisplayPort 1.3 supports 4K UHD at 120 Hz, while HDMI 2.0 is limited to 60 Hz.

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DisplayPort Multi-Stream Transport (MST) lets you connect multiple displays with a single cable.

**Some Features of DisplayPort**

- **Interoperability**
  DisplayPort is backward-compatible with DVI, Dual Link DVI, VGA, and HDMI displays, featuring some of the most extensive levels of interoperability of any display interface. By adding legacy adapters, users can retain their older displays even after upgrading to PCs that have already phased out the older display interfaces. This permits users to upgrade the display on their own terms.

- **Daisy-chain**
  DisplayPort Multi-Stream Transport (MST) lets you connect multiple displays with a single cable. The total number of monitors that may be daisy-chain depends on the resolution of the signal from the video output and the DisplayPort version.

- **Royalty-free**
  DisplayPort is an open and royalty-free standard, while HDMI charges each high-volume manufacturer an annual fee of about $10,000, as well as a royalty of $0.04 to $0.15 per unit.

**DisplayPort Future-Proofs**

Beyond 4K UHD displays

With technology standards changing as rapidly as they have, the two key components ensuring long-term feasibility are capability and backward compatibility. The DisplayPort standard accomplishes both.

Given that 4K monitors have just begun to breach the mainstream consumer market, it may come as a surprise that the DisplayPort was able to support 4K resolutions at 60 Hz with full 30-bit 4:4:4 colors as early as 2010 (DisplayPort 1.2). Its successor, DisplayPort 1.3, further improves bandwidth rates from 17.28 Gbits/s to 32.4 Gbits/s (four lanes), raising 4K UHD monitor refresh rates to 120 Hz with full 24-bit 4:4:4 color or 96 Hz using 30-bit colors. This is important from a graphics-intensive perspective, because the refresh rate is the bottleneck governing the maximum frame rate.

The cost of sustaining 60 FPS at 4K and 4K UHD resolutions under high settings is unrealistic with current computer hardware, let alone 120 FPS. But this will certainly change within the next few generations of video cards, which is why it’s important to have a video-to-monitor output standard that can capably leverage future upgrades.

At present, HDMI 2.0 is the only other standard with enough bandwidth to deliver 60 Hz, but it’s a nascent standard with minimum implementation. By the time HDMI 2.0 will have disseminated across the wider spectrum of consumer electronics, it will already have been surpassed by DisplayPort 1.3, a standard able to support 5K resolution at 60 Hz and 8K resolution at 30 Hz with 24-bit RGB color.

When the new HBR3 link rate becomes available for production, DisplayPort 1.3 will push 8K up to 60 Hz. In the meantime, though, DisplayPort 1.2 will perform the same function as HDMI 2.0, but with wider integration and a larger data bandwidth.

DisplayPort 1.3 supports audio and 3D Stereo

The multi-channel nature of DisplayPort ensures it can transmit both audio and video data using a single cable. Furthermore, the standard includes protocol support for transmitting stereoscopic data for 4K 3D graphics.

Legacy interface compatibility

While DisplayPort was originally intended to have its own specific connector, VESA manages a DisplayPort Compliance program to ensure the standard’s interoperability complies with millions of other displays, using connectors with both digital-to-analog and digital-to-digital converters. First and foremost, the latest DisplayPort version is always backward-compatible with earlier versions, so the release of DisplayPort 1.3 does not make DisplayPort 1.2 products obsolete.

Standards like VGA, DVI, and HDMI are supported through third-party connectors, so product designers will want to minimize time-to-market by taking advantage of well-established reference designs that provide layout guidelines to help optimize performance and lower EMI, as well as aid interoperability. A number of IC makers have DisplayPort interface ICs, including NXP, Texas Instruments, STMicro, Pericom, IDT, and Maxim.

STMicro’s STDP9320 chip combines a DisplayPort 1.2 transceiver, an HDMI 1.4 receiver, and a dual DVI receiver with WQXGA (2,560 x 1,600) 60-Hz performance. NXP offers level shifters, multiplexers and adapters to support the trend to DisplayPort interconnectivity; they have several families of parts to address conversion to DP. Their reference designs for DP-DVI, DP-HDMI, and DP-VGA adapters use the PTN3380, PTN3381, and PTN3392 ICs. For example, the PTN3392 DisplayPort-to-VGA adapter has integrated flash supporting resolutions up to WUXGA (1,900 x 1,200, 60 Hz).

Texas Instruments’ single-chip DockPort controller, the HD35S2521, provides a lower-cost alternative to proprietary implementations and offers more features than standard USB docking stations do. The controller enables DisplayPort, USB 3.0, USB 2.0, and power over a single interconnecting cable. It also provides the control logic and automatic switching required on the cable’s host and dock sides.

The multi-channel nature of DisplayPort ensures it can transmit both audio and video data using a single cable.
Most PC manufacturers offer DisplayPort interfaces, and Intel makes a line of small box computers, called the NUC, that have a mini-DisplayPort output.

While DVI and VGA remain the most widely supported computer monitor standards, DisplayPort is set to replace them with the onset of high-resolution displays. Meanwhile, HDMI’s specific qualities ensure that it will remain mostly in consumer electronics such as televisions, Blu-ray players, gaming consoles, and set-top boxes.

**Cables**
One drawback to HDMI is that there are too many cables and that using the wrong one can result in artifacts, visual and audio glitches, synchronization issues, or degraded performance. As of HDMI 1.4, the total number of cables had been consolidated to five:

- Standard HDMI Cable: Limited bandwidth cannot surpass 720p and 1080i video resolution.
- Standard HDMI Cable with Ethernet: Same as the above, except with 100-Mbps Ethernet.
- Standard Automotive HDMI Cable: Also supports 720p/1080i, but features a stronger signal than other cables for automotive systems.
- High-Speed HDMI Cable: Enough bandwidth for 1080p resolution, 4K resolution, and stereoscopic 3D at 1080p. The color depth and refresh rate differ depending on the standard (HDMI 1.4 or 2.0).
- High-Speed HDMI Cable with Ethernet: Same as the above, except with 100-Mbps Ethernet.

Among other factors to consider, HDMI output signals can only be converted to VGA or DVI, but input from VGA, DVI, Component, Composite, and USB may be converted to HDMI. There is no specific maximum cable length, but HDMI signals are subject to interference at longer lengths. HDMI Licensing LLC says that cables have passed compliance testing at lengths of up to 10 meters.

DisplayPort cabling is a much simpler matter; signals are transmitted through a single proprietary cable or USB Type-C. The cables are backward-compatible with previous standards, and the maximum length bandwidth for carrying to full bandwidth is only 3 meters, limiting its application in home theater set-ups.

**Data bandwidth**

- **HDMI 1.4:** The widely prolific HDMI 1.4 has an effective bandwidth of 10.2 Gbits/s, allowing it to provide 4K resolution at up to 24 Hz and 8 bits of color, or 16.7 million colors.
- **HDMI 2.0:** Released in 2013, HDMI 2.0 is still in early adoption. It raises the bandwidth to 18 Gbits/s, enabling 4K resolution at 60 Hz.
- **DisplayPort 1.2:** Released in 2009, DisplayPort 1.2 features a 17.28-Gbits/s bandwidth that permits 4K resolution at 60 Hz.
- **DisplayPort 1.3:** Launched in September 2014, DisplayPort 1.3 has not yet caught on. It raises the bandwidth to 32.4 Gbits/s, enabling 4K UHD at 120 Hz, 5K at 60 Hz, or 8K at 30/60 Hz.

**Daisy-chain**
Without taking into account any limitations imposed by the GPU, the number of monitors permitted in a daisy-chain setup depends on the display standard. According to VESA, a single DisplayPort 1.3 or 1.2 interface can support the following:

- Two 4K/4K UHD (3,840 x 2,160) displays at 60 Hz / One 4K/4K UHD display
- Up to four 2K displays (2,560 x 1,600) / Up to two 2K displays
- Up to seven 1080p or 1,920 x 1,200 displays / Up to four 1080p or 1,920 x 1,200 displays

HDMI 1.4 can drive only a single video and audio stream at a time per port, and there are no TVs or monitors that can echo a signal over another HDMI port; instead, screen space can be extended by using another port from the GPU with an HDMI adapter.

**Audio channels**
Both HDMI and DisplayPort include 8-channel audio with sampling rates up to 24 bits, 192 kHz.

DisplayPort delivers unrivaled flexibility capable of providing long-term future-proofing against the inevitable fruition of 4K and 8K.

**IN CONCLUSION**
DisplayPort delivers unrivaled flexibility capable of providing long-term future-proofing against the inevitable fruition of 4K and 8K. Its legacy interface compatibility ensures users will not have to simultaneously upgrade their PC and monitor. At the same time, the additional bandwidth is better reserved for gaming and other applications that rely on a high number of frames per second, whereas television viewing is better reserved for lower FPS, making HDMI 2.0 a more-than-adequate solution.

DisplayPort is technically able to fulfill both functions without imposing the same bottleneck as HDMI on any one particular application.
DDR4 LRDIMMs
Let You Have it All

LRDIMMs provide a superior alternative solution for both deeper memory and higher data bandwidth

Traditionally, LRDIMMs and RDIMMs have provided complementary solutions for data center enterprise servers—LRDIMMs for applications requiring deeper memory and RDIMMs for applications requiring higher data bandwidth. However, with the introduction of 8 gigabit (Gb) DRAMs, this white paper shows that LRDIMMs provide a superior alternative solution for both deeper memory and higher data bandwidth. In particular, 32 GB 2RX4 LRDIMMs based on 8 Gb DDR4 DRAMs are shown to transcend 32 GB 2RX4 RDIMMs in both server memory capacity and bandwidth.

By Douglas Malech and Sameer Kuppahalli, IDT and Ryan Baxter and Eric Coward, Micron Technology, Inc.

Endorsed by HP Server Architecture Team
The Need for Both Deeper Memories and Higher Data Bandwidth

There are a growing number of Internet applications benefitting from both deeper memories and higher data bandwidth such as in-memory databases (IMDBs). Larger IMDBs mean that more data can reside in high-speed DDR4 DRAM memory, reducing data exchanges with slower storage media during data processing. Reducing data exchanges with slower storage media means the memory-intensive application will run faster. IMDB application examples include data analytics, financial algorithms, gaming and search algorithms. Figure 1 shows some examples.

The LRDIMM Advantage

Prior to 8 Gb DRAMs, 32 GB LRDIMMs were constructed using more expensive DDP, Figure 2. In 32 GB 4RX4 LRDIMMs based on 4 Gb DRAMs, two DRAM data loads from the frontside DDP and two from the backside DDP share the same data bus. These four DRAM data loads are further reduced down to one data buffer load by the LRDIMM’s unique data buffering architecture.

Because of this data load reduction technique, when populating three LRDIMMs in a memory channel, only three loads are present. In addition, the nine data buffers are physically located very close to the edge connector, reducing data transmission stub length. Reducing transmission stub lengths and stub counts improve signal integrity. Figure 3 shows a memory controller channel (MCH) configured with three LRDIMMs (3 DPC). Improving signal integrity adds more signal margin, thereby improving server system reliability when populating thousands of memory modules into thousands of servers at a typical data center.

Contrary to 32 GB 4RX4 LRDIMMs, 32 GB 4RX4 RDIMMs were not developed because, in the absence of load reducing data buffers, all four DRAM data loads would be visible to the MCH channel, presenting twelve loads in a three RDIMM per MCH configuration (4 DRAM loads x 3 RDIMMs). In addition, without data buffers, the signal distance from the DRAMs to the edge connector is increased. An increase in transmission stub lengths and stub counts means poorer signal integrity. This is why RDIMMs based on 4 Gb DRAMs stop at 16 GB 2RX4 memory capacity while LRDIMMs go up to 32 GB 4RX4 memory capacity.

As applications continue to benefit from increased memory capacity, 8 Gb DRAMs enable the RDIMM “sweet spot” to increase from 16 GB memory modules to 32 GB. A 16 GB RDIMM is constructed using 4 Gb DRAMs in a 2RX4 configuration. It follows that a 32 GB RDIMM can be constructed from 8 Gb DRAMs using the same 2RX4 configuration because each DRAM contributes twice as much memory. Likewise, a 32 GB LRDIMM can be reconstructed using 8 Gb DRAMs in a 2RX4 configuration instead of using more expensive DDPS in a 4RX4 configuration. With 8 Gb DRAMs doubling RDIMM memory capacity from 16 GB to 32 GB and simultaneously replacing more expensive DDPS previously used to construct 32 GB LRDIMMs, which is the better choice for fully populated systems—32 GB LRDIMMs or 32 GB RDIMMs? Our lab measurements show that 32 GB 2RX4 LRDIMMs have a clear advantage over 32 GB 2RX4 RDIMMs in that you can benefit from the additional memory at a higher bandwidth.
Comparing 32 GB LRDIMMs and 32 GB RDIMMs

A typical enterprise class server can have up to 24 memory modules as shown in Figure 4. A server with 24 memory modules, each with 32 GB of memory, will have 768 GB of memory (24 x 32 GB).

IDT wanted to see which 32 GB memory module solution provided the superior solution for both total server memory and data bandwidth —LRDIMM or RDIMM. The process by which IDT made this determination was in the following manner:

1. Determine the module’s signal integrity on the MCH channel for the fully populated 3 DPC system configuration

2. Choose the highest speed possible for LRDIMM and RDIMM with acceptable signal integrity.

3. Compare bandwidths at these highest speeds to determine whether LRDIMM or RDIMM gives higher memory bandwidth

Data Signal integrity was measured in two places as shown in Figure 5 as V+ and V-. More positive V+ and more negative V- voltage measurements infer better signal integrity. In each case, it is a measure of how much voltage margin is available between the actual Data Eye Signal and the Data Eye Mask. The Data Eye Signal must never dip into the area within the Data Eye Mask for all combinations of data signal patterns, DIMMs, server motherboards and microprocessors. If the Data Eye Signal dips into the Data Eye Mask region, a data value of “1” might be interpreted as a “0” and vice versa.

The four measurements taken for receive and transmit directions show that 3DPC LRDIMM signal integrity at 2400 MT/s operation has better signal integrity than 3DPC RDIMMs at both 2400 MT/s and 2133 MT/s speeds. The measured signal integrity data is shown in Figure 6 with the 3DPC RDIMM measurements in AMBER and the 3DPC LRDIMM measurement in GREEN. LRDIMM at 2400 MT/s has more positive V+ and more negative V-, indicating overall better signal integrity.

<table>
<thead>
<tr>
<th>DPC Speed</th>
<th>V- (mV)</th>
<th>V+ (mV)</th>
<th>V- (mV)</th>
<th>V+ (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 2133</td>
<td>-173</td>
<td>164</td>
<td>-156</td>
<td>156</td>
</tr>
<tr>
<td>2 2133</td>
<td>-117</td>
<td>122</td>
<td>-125</td>
<td>125</td>
</tr>
<tr>
<td>3 2133</td>
<td>-66</td>
<td>70</td>
<td>-70</td>
<td>70</td>
</tr>
<tr>
<td>1 2400</td>
<td>-159</td>
<td>159</td>
<td>-133</td>
<td>133</td>
</tr>
<tr>
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<tr>
<td>3 2400</td>
<td>-51</td>
<td>64</td>
<td>-79</td>
<td>79</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>DPC Speed</th>
<th>V- (mV)</th>
<th>V+ (mV)</th>
<th>V- (mV)</th>
<th>V+ (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 2133</td>
<td>-173</td>
<td>164</td>
<td>-156</td>
<td>156</td>
</tr>
<tr>
<td>2 2133</td>
<td>-108</td>
<td>98</td>
<td>-156</td>
<td>156</td>
</tr>
<tr>
<td>3 2133</td>
<td>-84</td>
<td>94</td>
<td>-117</td>
<td>117</td>
</tr>
<tr>
<td>1 2400</td>
<td>-164</td>
<td>159</td>
<td>-140</td>
<td>148</td>
</tr>
<tr>
<td>2 2400</td>
<td>-122</td>
<td>117</td>
<td>-140</td>
<td>148</td>
</tr>
<tr>
<td>3 2400</td>
<td>-80</td>
<td>84</td>
<td>-101</td>
<td>109</td>
</tr>
</tbody>
</table>

Figure 4.

Figure 5.

Figure 6.
Since 3DPC RDIMMs at 2400 MT/s had much lower voltage margins, IDT assumed that this RDIMM combination of speed and density would be ignored as a possible candidate for server applications. While 3DPC RDIMMs at 2133 MT/s also showed lower voltage margins, IDT chose this 2133 MT/s speed configuration, in absence of the 2400 MT/s option, to compare bandwidths with 32 GB LRDIMMs operating at 2400 MT/s.

IDT used Membw2 to compare bandwidths. Membw is a memory bandwidth testing software package that is public domain software. Membw stresses the memory modules with reads and writes across all memory channels. The server configuration used in this benchmarking exercise has two Intel multi-core microprocessors, each with 4 memory channels and 3 DPC for a total of 24 memory modules.

The Membw benchmark measurements showed that 3DPC LRDIMM bandwidth at 2400 MT/s is 8% higher than the 3DPC RDIMM bandwidth at 2133 MT/s.

Evolving enterprise server applications will benefit from both higher bandwidth and more memory module capacity. IDT compared 32 GB 2RX4 LRDIMM and 32 GB 2RX4 RDIMM performance in a 3DPC configuration for both signal integrity and read/write bandwidth. A fully populated server with 24 32 GB LRDIMMs operating at 2400 MT/s showed better signal integrity than the same configuration using 24 32 GB RDIMMs operating at 2133 MT/s. The LRDIMM operating at 2400 MT/s also has an 8% higher bandwidth than RDIMMs operating at 2133 MT/s.

DDR4 LRDIMMs let you achieve higher memory bandwidth than RDIMMs at even mainstream module densities.

<table>
<thead>
<tr>
<th>3DPC, 2Rx4, 32GB modules</th>
<th>RDIMM</th>
<th>LRDIMM</th>
<th>% improvement with LR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Speed (MT/s)</td>
<td>2133</td>
<td>2400</td>
<td>13%</td>
</tr>
<tr>
<td>Measured Bandwidth (GB/s)</td>
<td>125</td>
<td>135</td>
<td>8%</td>
</tr>
</tbody>
</table>

Figure 7.
Open-Silicon Provides Complete Semiconductor Solutions from Concept to Production

System and product original equipment manufacturers (OEMs) can use all the help they can get these days to get their products to market quickly and flawlessly. Consumers are placing significant pressure on OEMs, as the demand for data and processing power exponentially increases in devices they manufacture. The increase in the flow of information from the Internet of Things and connected devices has put additional requirements on the infrastructure that service providers have to deal with. While OEM design budgets are spread thin, companies like Open-Silicon see an opportunity to aid in the development of processing power by providing design and development resources at the application-specific integrated circuit (ASIC) level. This model allows customers to architect products that meet the consumer demands and hand them off to a company like Open-Silicon to take advantage of streamlined chip design implementation and production process. This model has resulted in the shipment of over 110 million ASICs to date at Open-Silicon, with no end in sight. EEWeb spoke with Taher Madraswala, CEO of Open-Silicon, about the company’s unique platform and the future of ASIC development in the industry.

Interview with Taher Madraswala – President and CEO of Open-Silicon
How did the idea behind Open-Silicon come about?

The idea came about when we found a new way to make ASICs more affordable. In early 2000, infrastructure-related ASICs would typically cost around $1,000 to $2,000, which were very expensive for many system developers to adopt. When we sat down to determine why the ASICs were so expensive, we found a gap in the ASIC business model that we were able to exploit. Our plan was to charge a nominal fee upfront so that everybody pays for the development cost irrespective of who became successful with their idea. This took away a need to amortize the cost of failures over the successes. This allowed people to translate ideas to build a custom piece of hardware into real products by leveraging economies of scale for chip design and manufacturing, which is what a company like Open-Silicon provides.

That’s the gap that we saw in the business model in 2003 when we started Open-Silicon. Our main goal was to make ASICs affordable and to find ways to reinvigorate the industry by employing custom designs so that they can differentiate themselves in the solutions they provide at the hardware level. We trained an engineering group with state-of-the-art design methodologies and decided that we would keep the technical solutions open by listening to the customers’ needs and then map their needs to available pieces of IP at any given IC foundry so long as we were able to solve a customer’s price-performance equations. Since then, we believe we have made an impact on the industry—our presence has allowed the community to build affordable ASICs.

What are some of the different ways that Open-Silicon works with its customers?

If you look at the industry at different time stamps, the chip manufacturing business started becoming fabless around the turn of the century and the foundries consolidated as the cost of building new foundries increased significantly. In recent years, the cost of building in-house engineering expertise has started to rise. I have been sharing my views with GMs who are in charge of product development, and asking them to think about whether it is in their interest to invest in a design group with design tools to do one chip every year. We have offered the industry a way to outsource the design to help cap engineering costs without having to reduce the number of projects. Because we do so many designs across so many technology nodes every year, we have become experts at translating a netlist into a layout, or translating an RTL into a layout—while maintaining the needs of the OEMs to introduce new products every year.

Can customers come to you with a varying scale of production needs—from one-off designs to thousands of designs?

Yes, they can. We expect customers to come to us at an idea level, without having the detailed expertise of the technical needs of the project. We have...
Our competitors. Differentiation from and that is also our engagement levels. We work at all supply tested parts. We work at all designs from the RTL level or the netlist level. It has been my philosophy from the very beginning that we have to listen between the hardware and the software. These customers come to us and we take it from that point to design and manufacture the parts for them and they already know the problems. Customers come to us and they already know the problems between the hardware and the software. Sometimes our customers have already gone through the micro-architecture of the device and they already know the problems. We do not believe that an increase in complexity should directly translate into an increase in resources required to do the job because improvements in design practices should help us improve productivity to limit the number of hours needed to finish a project.

Customers like the option of taking the investment that would go into hiring and maintaining a design team for one chip a year and giving a part of it to a company that can amortize the cost over 10 to 15 chips a year. Just from this scale, we have the ability to learn and always be ahead of the curve and help customers take care of the silicon design and manufacturing. Customers have already gone through the micro-architecture of the device and they already know the problems. Sometimes our customers have already gone through the micro-architecture of the device and they already know the problems.

We work at all engagement levels and that is also our differentiation from our competitors. Most of our competitors will only take designs from the RTL level or the netlist level. It has been my philosophy from the very beginning that we have to listen always and add value at everything we do to solve a customer’s need—which is our core guiding principle for success.

What has been some of the customer feedback from this model?

In our industry, the cost of manufacturing transistors has gone down over the years, whereas the cost of designing silicon has gone up because complexity has increased. Our effort has been to manage this increase in complexity. We do not believe that an increase in complexity should directly translate into an increase in resources required to do the job because improvements in design practices should help us improve productivity to limit the number of hours needed to finish a project.

Customers like the option of taking the investment that would go into hiring and maintaining a design team for one chip a year and giving a part of it to a company that can amortize the cost over 10 to 15 chips a year. Just from this scale, we have the ability to learn and always be ahead of the curve and help customers take care of the silicon design and manufacturing while they spend a lot more time on application software, marketing and talking with their customers to find out what they will need a few years down the road. The customer can then articulate those needs back to us to help us develop an architecture that fits those needs. We have the advantage of leveraging our experience across several ASICs, which becomes very appealing to a lot of our customers.

What are some of the challenges that the semiconductor industry faces?

Lately, the biggest challenge affecting the semiconductor industry is that the funding for new ventures is drying up. Unfortunately, those who spend money and take risks in the semiconductor industry are now putting a lot more money on the software side than on the hardware side. The other challenge is how to justify the spending in bringing such complex devices into the market. I’m sure as we go from the 16nm process to 10nm and below, more of the manufacturing challenges will translate into design challenges. This will put a lot of pressure on designers to make sure that the devices are laid out in the correct orientation as the layout rules become much tighter. Designers must be more careful when they are laying out transistors to ensure that the device is manufacturable. FinFETs, and double/triple patterning methods applied during manufacturing, will require new sets of tools to design correctly.

Companies like Open-Silicon foresee these challenges and we have the ability and the desire to invest in, and overcome, those problems ahead of time. We spend significant R&D dollars to solve such design issues by working directly with tool vendors and partners so that the customer won’t have to solve them. The cost of doing ASICs is also increasing.

When we look at the ASIC itself, and break it up into parts, normally it will have an embedded processor, standard interfaces and a custom data processing engine. As consumers push the industry toward more video capabilities and more connections between devices start to happen, the data on the network will increase exponentially. All of this data will have to be processed in real-time via silicon. The processing needs will skyrocket and the need for low-power processing will also increase. The industry will have to solve this problem by dividing the design into two parts—a low-speed ASIC part and a high-speed ASIC part. This will result in acceptance of 2.5D and 3D packaging solutions where we can assemble these two ASIC parts back again on a silicon interposer and create a system-in-package (SIP). This will eliminate the need to have all of the silicon done on the more advanced and expensive technology nodes. The industry is already working toward solving those issues, and Open-Silicon is leading that effort along with our partners.

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