OCTOBER '15
Building Differentiated Products
New Ultra-flat GDT Technology
PCB Prototyping Made Easy
Bay Area Circuits’ Unique Process Technology Gives Engineers the Full Package
Interview with Stephen Garcia
President of Bay Area Circuits

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New Ultra-flat GDT Technology
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Building DIFFERENTIATED PRODUCTS Through Shorter, More Predictable DESIGN CYCLES

To position themselves for growth in today’s market, systems companies need to build highly differentiated products; reduce time to market; and focus on compliant, environmentally aware designs. This article addresses the first two challenges—the needs to build differentiated products and reduce time to market. It also discusses new design techniques, processes, and methodologies that can reduce design cycles by as much as 40-percent.
This article will focus on the first two challenges: building differentiated products, which can enable systems companies to quickly penetrate a market, take a leadership position, and effectively counter or displace any competition; and building them faster. Clear differentiation also allows a superior value proposition, which will enable a stronger position on pricing with less need to succumb to eroding ASPs. Differentiation can involve many factors, but this paper will focus on those related to the technology impact /usage that directly enables the design of products with shorter, more predictable design cycles compared to the competition.

NEEDS EVOLVE WITH NEW DEVICES AND ARCHITECTURES

Ever since design automation tools were invented, the EDA mantra has been shorter design-cycles. First, EDA tools were compared to an Etch A Sketch, and then they were compared to themselves—previous generation tools and methodologies. So, should every release of the software just be compared to its previous version? The answer, obviously, is no. The most important comparison of a particular release of EDA vendor’s software is to compare it to the user’s / company’s design needs—i.e., How well does the new release of the PCB or IC packaging software address the design challenges the end users have?

A company’s design needs evolve as the products and services a company offers evolve. Every company wants to differentiate its offerings from its competitors, and get its products to market faster, cheaper, and with more functionality. Systems companies are also impacted by new ICs and design methodologies offered by the semiconductor industry. A good example is the introduction of serial links—such as PCI Express® , Serial ATA—which change the architecture of signals on PCBs from parallel interfaces to serial interfaces. Another good example is the increasing capabilities and capacities of FPGAs, which shorten the design cycle time for system designers but add additional design challenges (pin assignment time, and increased number of iterations between PCB layout designer and FPGA designer). Pressures to reduce development costs while shortening design cycles have been forcing many companies to use low-cost geographies to do PCB designs.

Semiconductor companies often introduce new devices, interfaces, and architectures that are intended to help their systems company customers in shortening the design cycle or offering improved performance. Since their ROI lies in developing solutions that apply to the majority (not just the early few), EDA vendors and their tools tend to lag adoption of such new interfaces and architectures. When such changes are driven by standards, EDA companies can be sure that changes they make to support new interfaces—such as DDR3, DDR4, PCI Express Gen3, USB 3.1 etc.—will be applicable to a broader customer base.

When there is a need that is not supported by EDA vendors, many companies customize and/or extend EDA vendors’ tools to address their immediate needs while they wait for their EDA vendors to catch up and fill the gap. In such cases, end users need a system that is easily extensible and an EDA vendor that supports end users’ abilities to extend and customize the tool capabilities quickly and reliably.

Sharing your long-term design challenges roadmap (not your end product roadmap) makes your vendor a partner, and often allows appropriate roadmap alignment to address your needs sooner, rather than later. You should have an ongoing communication with your partner/ vendor on what and how future releases being developed helps you to get what you need to shorten your design cycle.

WAYS TO ACHIEVE SHORTER, MORE PREDICTABLE DESIGN CYCLES

How do PCB and IC packaging customers shorten their design cycles? There are several ways companies achieve shorter, more predictable design cycles. Although approaches vary depending on the size of the company, the market segment that the company belongs to, and its competitive position within that market segment, here are some common themes:
Eliminate Unnecessary Design and Physical Prototype Iterations

Deploy a Constraint-driven Design Flow

All EDA systems provide a way for incorporating traditional design manufacturing rules. Over the years, such systems have evolved to provide real-time feedback on such traditional rule adherence as the design is created and manipulated. This is the baseline. With the introduction of new devices and architectures, new design rules have to be followed. For example, using differential pairs provides some electrical advantages; they also introduce additional rules for physical implementation of such signals. Rules required to route serial links such as PCI Express Gen2 versus rules required for parallel interfaces such as DDR3 and DDR4 are very different. Often a system these days includes both serial and parallel interfaces. Having a system that allows you to specify all the rules for all such signals on your board is important. Similarly, as the manufacturing process for your designs evolves, you need a system that can combine such new rules for both manufacturing and electrical domains and guide the design as it is being developed. Having an iteration at the tail end of the design cycle—either for lack of electrical rules adherence or for lack of manufacturing rule adherence—makes the design cycle long and, worse, unpredictable.

Develop constraints through simulation to enable a constraint-driven design flow. This involves using solution space exploration to ensure development of optimal constraints for your design—these constraints, in turn, ensure that your product performs at its peak in various operating conditions. This upfront investment helps avoid iterations at the tail end of the design cycle, which could make it harder to predict when the design will be completed.

The cost of not developing such a constraint-driven design flow can either lead to several physical prototype iterations with debugging in the lab or, worse, customers finding problems with your design. The cost of physical prototype iterations varies among customers in different geographies; time lost in doing an iteration ranges from two to six weeks. Investing some of this time from one physical prototype iteration is, in and of itself, sufficient to enable a constraint-driven design flow.

Use a Constraint-driven Flow that supports HDI designs

Many customers are being forced to use High Density Interconnect (HDI) technology to fanout small pin pitch BGAs. BGAs with pin pitches of 0.8mm or lower usually require HDI build-up layers for fan out. A constraint-driven design flow must integrate HDI manufacturing rules with electrical rules and traditional manufacturing rules together to ensure that the design is being built correct-by-construction. Checking for fabrication rules after the design has progressed to the very end only increases the number of iterations between the tail end of the design process and doesn’t make the design cycle predictable. The solution is to use a constraint-driven flow that supports HDI designs.

Benefits of Deploying a Comprehensive Constraint-driven Design Flow:

- Improved product performance and chances of first-pass success through optimum constraints. Optimum constraints are developed through explorative simulation. Upfront development of such constraints enables and drives the constraint-driven design flow.
- Reduces time-consuming post-layout simulation to a post-layout verification step. With simulation-developed constraints that drive the constraint-driven flow, the post-layout simulation step now becomes a post-layout verification. This shortens the time required to get the design to manufacturing.
- Eliminates unnecessary physical prototype iterations. This shortens design cycle time and reduces product development costs.
- Design cycles become predictable.
I nnovation in the design authoring space now allows engineers to author designs using multiple styles—table-based for large-pin-count devices, schematics for traditional circuits with small-pin-count devices.

Accelerated Design Authoring

Design authoring has traditionally been associated with creating schematics in the EDA world. Additionally, in many instances the schematics created for simulation tend to be different than the ones used for driving the PCB layout process. Innovation in design authoring in recent years allows system designers to avoid having to author designs the same way engineers created them in the 1980s.

Design architectures have evolved since the 1980s from a common clock architecture to one that uses source synchronous interfaces (DDR3/4) and serial links (PCI Express, SATA). At the same time, with larger scale integration possible with each new advanced IC node, many FPGAs and ASSPs have far more pins than ever imagined—devices with greater than 1000 pins are becoming commonplace. Adding these large-pin-count devices on a PCB requires them to be added as a symbol in the schematics. Schematics often use company-defined sheet sizes. Fitting a 750-pin or even a 500-pin symbol is impossible in the standard sheet. Engineers and librarians are forced to represent such large-pin-count devices as multiple split symbols with labels to specify connectivity. Such split symbols are totally useless on the schematics.

Innovation in the design authoring space now allows engineers to author designs using multiple styles—table-based for large-pin-count devices, schematics for traditional circuits with small-pin-count devices. Such approaches can shorten the design authoring time significantly—in case of backplane designs, anywhere from 10X – 20X faster than traditional schematic creation. Time to create designs with large-pin-count devices (FPGAs or ASSPs or ASICs) mixed in with traditional circuits can be accelerated anywhere between 2X – 5X, depending on the number and size of large-pin-count devices. Use the right design authoring tool to shorten your design cycle.

For mixed-signal designs or for purely analog / RF designs, often engineers use two different schematic tools: one for simulation and another for production PCB flow. This implies someone is recreating the schematics for production PCB flow. Improvements in integration between design authoring tools and simulation tools—single schematic-driven design authoring and simulation—allow engineers to avoid wasting time to recreate schematics. For RF circuits on a mixed-signal design, engineers can use a layout-driven design approach to create schematics based on the changes made to the etch elements in the layout. This eliminates the need to edit schematics manually to synchronize it with layout.

Design for Reuse

A commonly used approach to shorten the design cycle is to reuse subsets of previous designs in new designs. Often, the next revision of a product is some modification that either reduces cost or adds some features that couldn’t be added with an earlier version—this is evolution of a product, not reuse of a subset of the design. For products that don’t fall into the evolution category, authoring the design in a manner that partitions functionality in a reusable manner can shorten the design cycle for other products. In such cases, the motivation to invest the time to partition and author designs for reuse has to come from upper management since the product team is usually focused on getting “their” product out the door quickly.

When a product has several design engineers working in parallel, such partitioning becomes a necessity and can be leveraged to create reusable blocks. Reuse can also be applied to the physical layout of the partitioned subset of the design. In such cases, it’s important to have a relationship between partitioned logic and its physical implementation. While the physical layout is tied to a specific layer stack-up, reusing the placement and etch should be easy. This reuse is referred to as a reusable block. Reusable blocks also have to deal with constraints that are embedded in the design and were used to guide the physical implementation. Such constraints can be very useful for the design engineer who uses a reusable block designed by another engineer. Engineers reusing such blocks should also carefully analyze the constraints on standard interfaces to see if any exceptions were made to the constraints to make that board work. In other words, if design-specific changes were made to make the block work in its original design, make sure that those exceptions will not create any issues in your new target design.

FPGA-PCB Co-design

FPGAs have grown in popularity over the years as their capacity and capabilities have increased significantly, while the cost-per-million equivalent system gates is going down with each new IC node. There are two categories of use for FPGAs: one is using FPGAs on end product PCBs; second is the use of FPGAs for ASIC prototyping boards. For both of these use models, integrating FPGAs on PCBs is a time-consuming effort. The first step in this process traditionally has been manual pin assignment using either the FPGA vendor tools (such as those from Xilinx or Altera), or in-house developed spreadsheet-based approaches. Once the pin assignment is done, integration with schematic is done manually. Pin assignment and integration is done one FPGA at a time, without much feedback from any tools on the quality of pin-assignment results from the routing the FPGA-on-board perspective.

You can also use an integrated FPGA-PCB co-design approach that brings PCB routing challenges into the pin assignment decision-making process. This automated approach should be done in accordance with the FPGA vendor’s pin assignment rules that optimizes the resource utilization of the FPGAs while improving the routability of FPGAs on board. This approach will reduce the number of frustrating iterations between PCB layout designer and FPGA engineer late in the design cycle.

Once the pin assignment is done, the integration of FPGA symbols in
schematics should be automated to reduce the time to integrate and avoid making any manual integration errors.

Divide and Conquer—Team Design
Divide and conquer approaches can be applied on both initial design-authoring stage as well as during the physical implementation—place and route—stages.

Team Design During Design Authoring
While having a team of engineers work in parallel shortens the design cycle, it also adds some design and process management challenges. Engineers working in a team while authoring the design have to deal with global signals and signals that interface to logic/circuit that is being designed by their colleagues. In such cases, using a signal-naming convention that is well understood and adhered to by all team members is important to avoid creating a problem that will only be caught during post-layout simulation or, worse, in debug stage in the lab with a physical prototype.

Another area to manage is when each engineer embeds constraints on nets in their designs. When the constraints are added to nets that are local in scope, things should work fine. Once constraints are added or modified on signals that interface with other engineers’ blocks, there has to be some level of management on who has the ownership to make such changes.

Often a system being designed has more than one fabric—either a combination of internally developed ASICs on a PCB or a system of multiple boards connected via a backplane or through cables. In such cases, managing interfaces that cross the fabric boundary has issues similar to the ones when multiple engineers work on a subset of the design targeted for one fabric—PCB or a system in a package (SiP).

Team Design During Physical Implementation
As the design complexities increase and design schedules shrink, one of the ways to shorten design cycle time is to partition the board among multiple PCB designers. This partitioning can be done vertically or horizontally. It is important that the design system allows you to manage the partitions and synchronization between the partitions automatically without slowing down your system or requiring IT support to enable partitioning.

Productivity and Ease of Use Improvements
This is an area that is common to all EDA tools. With every release of the software, there are improvements that help designers to be more productive. Productivity comes in many forms. The simplest involves automating some of the manual tasks. This applies to all areas of the tools. Earlier in the paper, we discussed one of the most fundamental productivity improvement capabilities—constraint-driven design. Included below are some examples of productivity improvements that shorten the design cycle and make it predictable.

Easy-to-use Intuitive Tools Help Shorten the Time to Create Designs
While this is very intuitive and self-explanatory, software products tend to lose their “ease of use” moniker as they evolve over a period of time. Often software that is very easy to use doesn’t scale well for larger, more complex design challenges. Software that is very flexible may be difficult to use. This is an area that needs to be addressed with every release of the software you adopt. Success also requires providing feedback to your vendor on an ongoing basis—not once a year—to help them incorporate improvements that make your design experience better.

A simple example of ease-of-use improvement is the ability to put vias with a single click for designs with hybrid HDI designs (HDI layers on each side of a non-HDI core). With traditional through-hole vias on a design, single click to place a via is the norm. With HDI layers around a non-HDI core, a system should allow users to instantiate multiple vias that are placed according to the rule specified with the user specifying the from to layer. This is a good example of how layout of HDI designs can be made easy even with a complex set of rules for advanced designs. Incorporating such new approaches allows users to shorten the time required to create their designs.

Auto-interactive Routing Technology
Decreasing pin pitches, greater numbers of large pin count devices, and the need to reduce the footprint all contribute to the increased challenges in planning and routing a dense PCB design. Additionally, as the PCB interconnect paradigm shifts to increased use of standardized source-synchronous interfaces (such as DDR3/DDR4) and serial interfaces (such as PCI Express), the number of constraints that must be adhered to increases. An example of a set of routing requirements for DDR3/4 interface is listed below.

Data bus requirements:
- Group and route data, data mask, and data strobe signals by byte lane
- Tightly match members inside of the byte lane
  » 20 mils between members
  » 5 mils differential pair phase tolerance
- It is not required to match lengths across all byte lanes. Length matching is only required within each byte lane.
- Byte lane members should be routed on the same layer and only use vias to escape from surface mount devices so routing can be done on an internal layer

Address / Command / Control Bus Requirements:
- Should be matched within +/- 10 mils
- Routing on the same layer is not required but referencing the same
of the work to meet complex timing constraints. Such an auto-interactive strategy can allow you to tune advanced through tuning and adjusting. Ideally, you’d drive the strategy and execution, but have the computer do the bulk
Additionally, you need a way to leverage the feedback from the system to tune differential pairs and meet timing
Figure 7: An example of how visual feedback on the design canvas avoids back-and-forth trips to the constraint manager.

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Accelerated Timing Closure

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To meet this increasingly complex challenge, you need an environment that allows you to graphically see real-time delay and phase information directly on the routing canvas – timing vision. Traditionally, evaluating current status of timing/length of a routed interface requires numerous trips to the constraint manager and as well as reviews of other current properties. What would be helpful here is a system to evaluate complex timing constraints and interdependencies amongst signals that show the current status of a set of routed signals—a DDRx byte lane or a

Figure 6: Reduce layer counts and shorten design cycle through design planning.

Traditional automatic routers have been unable to route such dense PCBs with high-speed interfaces that require strict adherence to constraints (often derived through simulation for optimum performance on the PCB).

To reduce the time to design such boards, you should do auto-interactive routing to not only capture, but adhere to, routing intent for dense designs with highly constrained, standards-based interfaces. After capturing design intent, use feedback from the tools on such planning to adjust your routing approach.

Memory interface general requirements:

- Signal ended impedance target: 50 – 600ohms
- Differential pair impedance target: 100 – 1200ohms
- All routing should be routed close to and have a solid reference plane to provide a low-impedance path for return currents
- To avoid any possible crosstalk between layers, develop a stack-up to utilize strip-line construction (reference plane above and below signal layer) instead of dual strip-line construction (two signal layers between reference planes)
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- Solution space exploration (multiple concurrent simulations) for signal integrity analysis of digital signals
- Parametric Monte Carlo analysis for analog signals
- Batch design rules check

Predictable and Reliable Release Schedule

Having a predictable and reliable new release schedule from your vendor allows you to plan adoption of such releases based on the value of the improvements promised. Migrating to a new release can be time-consuming, especially if you leveraged the ability to extend the base tools either through in-house developed extensions or by using third-party tools. An open architecture software platform that works in conjunction with third parties and a new release can be time-consuming, especially if you leveraged the ability to extend the base tools either through in-house developed extensions or by using third-party tools. An open architecture software platform that works in conjunction with third parties and a new release can be time-consuming, especially if you leveraged the ability to extend the base tools either through in-house developed extensions or by using third-party tools. An open architecture software platform that works in conjunction with third parties

Multi-core CPUs or Multi-CPU Machines

Most personal computers these days come with dual cores. Engineering workstations tend to have more cores in one CPU. Server farms have been around for quite a while where many machines are linked in a network for compute-intensive tasks. In either case, there are several applications that can benefit from leveraging multiple CPUs—whether they are housed inside one computer or in multiple computers. These applications include:

- Divide and Conquer II—Outsourcing

Over the years, many companies have outsourced PCB layout partially or completely to service bureaus. Many larger global companies have opened

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design centers in low-cost geographies like India and China. Such companies hope to get two days’ work done in one due to time differences.

Outsourcing opens up a new set of collaboration challenges for companies. In such cases communicating complete design intent is necessary. Complete design intent implies not just traditional connectivity (parts and how they are connected) but also the constraints that these parts and signals need to adhere to. Without communicating constraints, the design cycle becomes long, arduous and, worse, very expensive. The whole reason for outsourcing may be a wash if constraints are not embedded in the design.

Once the layout is completed and sent back for review and approval, two approaches need to be taken. First, verify if any of the constraints were modified for any reason (compromises have to be made: which ones were made and are you ok with it?). Second, do post-layout verification to ensure that the realized physical implementation will work within the boundaries that are acceptable to you.

**Use an Open Architecture**

An open architecture offers freedom to choose third-party tools. All vendors will claim to have an open architecture. Often you don’t find out how open the architecture is until it is too late. There are two ways that an open architecture helps shorten the design cycle.

The first is easy access to your design data for internal consumption or for use with third-party tools. Is your design data stored in a binary or an ASCII database? Is there a way for you to extract the information easily from the binary format without having to write any software? How easy is it for third parties to integrate their tools to your design data in the primary vendor’s format?

Having a way to extract the information you need for internal use—documentation, reports, etc.—can be very helpful and can shorten the time it takes on each project significantly. Many tools offer report generation, some are customizable. Being able to create your own quickly as the need arises helps you focus on your project/design instead of struggling with the tools and tool vendors.

The second way that an open architecture can shorten the design cycle is through tool extensibility for home-grown extensions. Does the tool allow you to customize the presentation layer (GUI, menus, etc.)? Does it allow you to add-in your extensions, whether they be for report generation or for a more serious application to fill in the gap while the vendor is catching up to your need? Being able to extend the system is important. In addition, the support for such extensions should not be consistent from release to release for 5-10-12 years. Such extensions should work with all the vendors’ tools—i.e. not have discontinuity as you move up to working with advanced designs, projects with advanced tools.

**SUMMARY**

In today’s environment, with increasing design complexity and continuous pressure to reduce the time to author and implement a design, you need to deploy all possible techniques and tricks to build a differentiated product quickly. At a minimum, you need to use a constraint-driven design flow in an open environment that avoids unnecessary design iterations or recreation of schematics, and allows teams to work effectively. New innovations like multi-style design authoring, global planning and routing, and FPGA-PCB co-design enable teams to create differentiated products much faster than possible with traditional approaches. Users of these technologies have reported design cycle reductions of up to 40%.

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HARDWARE DESIGN MADE EASY.

PCBWeb Designer is a free CAD desktop application for designing and manufacturing electronics hardware. The tool supports schematic capture and board layout, including integrated “click-to-order” manufacturing.

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Circuit Protection Components from Littelfuse

Meet Stringent Safety Standards

Designers and marketing executives are easily recognizable as the common faces of the electronic components industry, but there are certainly many other aspects of a successful company's operation that go into creating a truly leading presence in the market. The standards and certification process, admittedly not exactly the most prestigious or celebrated of the bunch, always looms as a critically serious but easily neglected part of the work of any components manufacturer. Luckily these days, there are dedicated specialists, people like Saad Lambaz of Littelfuse, Inc., working hard to ensure that standards are not only met well in advance but that the best possible requirements are in place and working as they should.

Although it may seem like a secondary consideration, in reality it stands as a fundamental requisite, and makes the difference between the industry’s followers and its leaders.
Having begun his efforts working for Underwriters Laboratories (UL), a familiar and ubiquitous safety certification company that plays a central role in required third-party certification processes for any legitimate supplier, Lambaz now uses his skills to represent Littelfuse, one of the biggest companies in the modern components game, as Global Standards Manager for the company’s Electronics Business Unit. As a representative to a number of industry committees and technical groups, he also works diligently to help ensure that the electronics industry’s biggest players are working as hard as possible to uphold industry standards to the highest degree.

As Lambaz explains, the essential task is not only to make sure that a design does what it is designed to do, but also that the design meets the standards that exist outside those application-specific requirements. With this specialized knowledge at his disposal, Lambaz makes it possible for Littelfuse to essentially put their products fully to the test against the industry’s standards, long before sending them off for official review. “Standards can be intimidating, especially when it comes to new areas and when trying to design a new product. It can be tough to manage the path through the many different standards and specifications,” he says. But still, he adds, the ability to do so completely and effectively makes all the difference. Having worked for an agency that is responsible for numerous standards, especially in North America, it’s much easier for Lambaz to know how things are going to work in the big-picture scheme of the standards certification process, and this, he implies, is the kind of expertise needed to effectively provide for any company’s long-term success.

Additionally, Lambaz points out, “a big part of my job is to be an active part of the committees and technical groups that set these standards, too, and to understand from the roots of the matter where the requirements come from and what they really mean to the market.” Perhaps unsurprisingly, standards from different parts of the multifaceted global market are often in conflict with one another, and attempting to comb through the dense catalogs of standards can be an intimidating task for someone out of their depth. “Trying to design a product that has to meet very different requirements is a huge challenge, and more often than not, the process will result in more than one product.” But, he interjects, that’s where the big-picture challenge stands, and why Lambaz considers it the most important duty for those in his position to “make that a little easier, to harmonize standards across the board.” Today, he says, the standards organized and put forth by organizations such as the IEC, or the International Electrotechnical Commission, do a pretty solid job streamlining things in the modern market and making it possible to meet the requirements of different or competing policies. But, with a wise sense of experience and anticipation, Lambaz feels that there is always room for improvement.

“We live in a global world,” Lambaz reflects, “so it’s becoming increasingly uncommon for bigger companies to settle for simply targeting one national or continental market. The global aspect [of the modern market] makes it essential to understand the nature of standards throughout the whole world, which is more an integrated network than ever before.” In such a world, it only makes sense that developments in standards in one place are sure to have far-reaching effects throughout the whole global network, whatever they may be, and the effect that these variables can have only highlights the necessity of diligent work in increasingly essential roles like those played by Mr. Lambaz.
In direct relation to Lambaz’s particular area of expertise at Littelfuse, the company offers some of the world’s current leading circuit protection components for use in hazardous locations (e.g., locations and areas where combustible concentrations of gases, vapors or dusts exist) in normal operation) by utilizing the “intrinsic safety” protection method. These intrinsically safe products and components, which are so named for having advanced safety features for a particular hazardous environment built into their systems, are not altered or fit into additional structures to make them safe but are rather designed for specific electrical fault that, if not controlled quickly, can cause thermal runaway. This may result in a component that reaches a high temperature, which is very hazardous, particularly in the presence of combustible gases or dusts. The solution is to use a fuse, which is an intentionally weak link designed to open the faulty circuit, thereby limiting the spark energy and surface temperature.

Intrinsic safety products and components are designed to meet the requirements of the industry. They are developed to be safe but are rather designed for specific applications and environments, as opposed to being modified to fit into additional structures to make them safe. These products and components are designed to prevent the propagation of electricity, igniting combustible atmospheres, and requiring no other means of protection.

Recently, Littelfuse introduced two fuses specifically for intrinsic safety needs in industrial applications, the PICO® 259-UL913 Series and the PICO® 305 Series. With these fuses, the typical risks for an explosive event are greatly reduced by a specially designed encapsulation layer that first, minimizes the temperature of the fuse in both normal and abnormal circumstances and second, seals the fuse from the surrounding combustible atmosphere. As Lambaz details, the company also prides itself on being able to provide these specialized components in a complete package, without requiring customers to undertake any further steps to offer the product in its finished form, ready for use in intrinsically safe equipment.

Littelfuse has a network of global resources. Lambaz points out, which allows the company to combine these usually separate steps into a complete package that saves customers time and cost. Highlighting the company’s pre-emptive attention to standards and certification, he states that “our knowledge of the certification process also gives us the ability to ensure that no further testing is required and that customers can expect the best possible results from third-party certification.” With few companies able to offer such a package, the company is considered by many to be a step ahead of the competition.

It’s safe to conclude that it can only be of great advantage for a company to take the time to understand, as Lambaz says, “the different requirements of comparable standards, their history, and any of the changes to the standards that can affect your products.” With exactly that kind of considerate scope at their disposal, it seems that the knowledge of end-product standards in their many forms and variations stands as something that is only slightly less fundamental than the basic engineering knowledge that allows a company to build products in the first place. These standards guide design and manufacturing from its most basic stages, and, naturally, the success of a company’s innovations is only truly measured by how well they meet the requirements of the industry. “At Underwriters Laboratories, it was very common to see products up for certification that had not met very basic requirements,” Lambaz recalls. “My advice is to take the time and learn as much as you can about standards that will be applicable to your product, long before it even reaches the third-party certification agency.” It’s that kind of philosophy that puts Littelfuse ahead of the competition.

Littelfuse has a network of global resources, which allows the company to combine these usually separate steps into a complete package that saves customers time and cost.
Breaking Out the BGAs

All grid array devices are, without question, an increasingly important aspect of printed circuit board design. While their benefits are numerous, they present the unique challenge of requiring an enormous amount of traces to originate in a small area underneath a device and then go all over the board without crossing traces. The most challenging aspect is getting those traces out from underneath the board, a process called creating a breakout or fanout. In the breakout, these traces are said to escape from underneath the board and come to the outside where they are more accessible. A poorly designed breakout can be overcome by increasing the layer count on a PCB but that increases the cost and complexity. There are number of different scenarios that would require different approaches to breaking out the traces, however, due to limitations in space, only the more common concepts and methods will be discussed here.
When approaching a BGA breakout, there are several key features to watch out for. Foremost is the pin count, or how many balls there are on the device. Equally important is the pitch between the different pins. As the pitch decreases, the space available to run traces starts disappearing and the approach both in the fanout and the types of vias changes. There are different patterns used as well that will affect how you break it out, whether the balls are in perfect grids, in an offset pattern, or if the pattern is different for different portions of the component, and if there are no pins in the center of the component. Finally, not dependent on the component, is the constraints given to you by your manufacturer. If you need more demanding constraints, you may need to look at a different manufacturer but that will cost more and there is a limit where even the most advanced manufacturers simply cannot go smaller.

Blind vias allow you to connect an outer layer with an inner layer without having to go entirely through the board. Through-hole vias are simple and inexpensive and they allow you to get your signal to any layer on the board you need. However, it also makes a hole all the way through all of the layers, so whether or not a via is attached to a certain layer, that spot on each layer is unusable. With this limitation, through-hole vias are really only feasible while working with BGAs up to a couple hundred pins. After that, it starts to become increasingly difficult until it is completely impossible to properly break out the BGA using through-hole vias with or without an astronomical number of layers.

A key part of actually fanning out the signals is the use of vias. Through-hole vias are simple and inexpensive and they allow you to get your signal to any layer on the board you need. However, it also makes a hole all the way through all of the layers, so whether or not a via is attached to a certain layer, that spot on each layer is unusable. With this limitation, through-hole vias are really only feasible while working with BGAs up to a couple hundred pins. After that, it starts to become increasingly difficult until it is completely impossible to properly break out the BGA using through-hole vias with or without an astronomical number of layers.

Blind and buried vias, while more expensive, greatly expands the capabilities of the board and allows for greater pin count while keeping the layer count reasonable. Blind vias allow you to connect an outer layer with an inner layer without having to go entirely through the board. Buried vias can connect two inner layers without affecting layers that are not between them. These free up a significant amount of space on the board and may save cost in the long run.

Once it is time to actually start designing the board, look into how the pins are set up. If there are general purpose IO available throughout the component and it is possible to choose the IO closer to the edge, do so. It is much easier to break signals out of the corners and sides of the component versus the center, so a proper setup will make your life easier. Also, in general, components have more of their power and ground pins in the center, so providing appropriate ground and power planes simplify matters by allowing vias to be dropped down directly to the planes. You will not be able to utilize that center space, but at least the effort of getting those signals out will not be necessary.

Two very common techniques that are used to fanout the different signals on a BGA. The north- south-east-west approach is very straightforward, easy to conceptualize, and works well with relatively small BGA components. In essence, take the traces out the side of the component that they’re closest to. A pin closest to the top of the component will have its escape trace go up toward the top. A pin closest to the left side of the component will go out that way. The other technique is the layer-biased approach, where all the signals on each layer tend to go a certain direction, either vertical or horizontal, until they are out from beneath the BGA. This is generally used with higher pin count devices that also require more layers to effectively route.
Done properly, you can create a board that will be inexpensive, powerful, and well balanced electrically. Done improperly, it could cost significantly more than it needs to be, be larger than it needs to be, and have serious ramifications to the performance of high frequency signals.

At the level of each pin, there are also two common ways to get the signal away from the pin itself. The dog-bone is so named because it looks like a dog bone. By creating a via away from the BGA pad, you decrease difficulties with soldering and can potentially increase spacing for the traces to be ran. The other common option is the via-in-pad, in which the via originates in the center of the BGA pad. This is useful as it doesn’t use any additional space on the outer layer, however, it presents solder wicking concerns and is thus discouraged by some manufacturers and assembly houses. When working on the design, it may be a good idea to contact your manufacturing chain and discuss with them their personal preference on the matter and see if the defect rate would make via-in-pad a non-viable option.

BGA breakouts is another step in the process of designing high quality circuit boards. Done properly, you can create a board that will be inexpensive, powerful, and well balanced electrically. Done improperly, it could cost significantly more than it needs to be, be larger than it needs to be, and have serious ramifications to the performance of high frequency signals. If delving into BGA design for the first time, it is recommended to find a mentor who can work with you and provide insight and feedback as well as looking deeper into written technical resources. The time and effort invested into learning how to do properly breakout a BGA will become even more valuable as time moves on and technology produces even smaller pitched, higher pin count components.

Advanced Assembly was founded to help engineers assemble their prototype and low-volume PCB orders. Based on years of experience within the printed circuit board industry, Advanced Assembly developed a proprietary system to deliver consistent, machine surface mount technology (SMT) assembly in 1-5 days. It’s our only focus. We take the hassle out of PCB assembly and make it easy, so you can spend time on other aspects of your design.

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While it is possible to use the solder paste layer gerber file as the basis for a stencil with a standard thickness, the result will be acceptable, at best, and at worst, completely unusable. However, spending time to refine and improve the basic solder paste design, as well as choosing the thickness and material, will result in a stencil that will consistently provide successful results.
By calculating how much paste will release on the terminations, versus how much will release on the ground pad, you can determine the correct opening size.

When designing stencil layouts, be careful to specify the solder mask thickness on the PCB fabrication drawings because the stencil has to print down below the mask to contact the pads. If the solder mask is too thick, the stencil will have contact problems.

The stencil design provides an opening of determined size and the thickness of the stencil is representative of the amount of paste that will be applied. Squeegees used with stencils often will be metal-pointed or wedge-shaped. Most stencils are used with semi-automatic printers, which provide the constant squeegee pressure and movement required for uniform results. The small apertures required by miniaturized components can push the limits of the area ratio rules, reducing them below the 0.66 threshold and reducing solder paste volume on the pad. Therefore, area ratios and transfer efficiency calculations are necessary, especially with small chip packages.

You will need to calculate the paste lay down volume with small terminations area ratio with a 5 mil foil stencil. By calculating how much paste will release on the terminations, versus how much will release on the ground pad, you can determine the correct opening size. Aperture openings for other components need to be enlarged if thinner stencil foils are used. You also need to calculate aperture size to maintain the same solder volumes and how much pad overflow that you will allow. New stencil design software can perform many different stencil design calculations and analyses. Area ratio and transfer efficiency (ARTE) can be used to find low flow areas, thus avoiding alignment issues. ARTE allows rapid changes of stencil design options, including changes in aperture size, shape or foil thickness, and predict lay down volumes of apertures. With ARTE software CAM imports, the stencil Gerber D file specifies a minimum area ratio threshold and selects a foil thickness. The software calculates the correct aperture volume and aspect ratio for each pad shape. The stencil design must account for PCB changes in size. On larger PCBs, final overall size can vary by up to .015 inches per 12 inches.

In surface mount assembly, the stencil is required to deposit accurate and repeatable solder paste. The solder paste brick holds the components in place so that when refloved, they are secured properly to the PCB. The stencil type, thickness and shape of its apertures will determine the size and position of the paste bricks, which is essential to ensuring a high-yield assembly process.

Design guide for stencil technology is determined by pad aspect ratio, which is defined as aperture width divided by stencil thickness and should be greater than 1.5.

Aspect ratio is a usable guide. Aspect is the difference in surface friction forces that either allows paste to flow from an aperture and onto a pad or causes paste to be held within an aperture. These forces can be calculated and are referred to as the aspect ratio. With the introduction of BGAs and QFNs, the aspect ratio has shrunk and is defined as the area of the aperture opening divided by the area of aperture walls. The walls of the aperture are trying to hold the paste in the aperture, while the pad under the aperture opening tries to pull the paste away after the squeegee passes.

If the aspect ratio is greater than 1.5 and the area ratio is greater than 0.66, you should have excellent print performance using a good quality laser stencil. During the printing process, as the stencil separates from the PCB pad, the surface tension forces determine whether the solder paste will stay on the pad or remain adhered to the stencil aperture walls. When the pad area is greater than 66 percent of the aperture wall surface area, the surface tension on the pad will improve paste transfer. As the ratio decreases below 66 percent, paste retention efficiency on the pad decreases and print quality becomes erratic.

It is recommended that finer pitch aperture openings be slightly smaller than the landing pad size. This is primarily for improved contact between the landing pad and the underside of the stencil, which prevents bridging on fine pitch component. Aperture width reductions must be taken equally from each side so that aperture is centered on the pad.

While other technologies are being improved that have faster setup times for small prototyping, stencils are a well-established and well researched technology that can yield great results with great repeatability. With a proper design, rework will be kept to a minimum and boards are most likely to receive the right amount of solder in the right locations.

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Working hard to forge the protective components that can keep today’s emerging technologies working at their best, Riverside, California’s Bourns, Inc. can be found playing a trusted role in an impressive variety of the modern world’s essential applications. A leading manufacturer and supplier of a range of products such as sensors, circuit protection devices, magnetic components, and resistive parts, Bourns is notably relied on by an impressive range of markets that includes the automotive, industrial, consumer, communications, and medical industries. With a history that begins with founder Marlan Bourns’ personal contribution to the Manhattan Project and progresses with the Apollo space program into a new era of modern technology, Bourns has been doing some very impressive things behind the everyday scenes.
Speaking with a panel of representatives from the Bourns Product Line Department, we learned a bit more about some of the recent work that the company has been doing in the circuit protection realm in particular. With a successful new line of aptly titled FLAT® gas discharge tubes (GDT) just released, we figured it was as good a time as any to find out what’s going on at Bourns, and we were certainly not disappointed.

As with much of today’s taken-for-granted technological infrastructure, many of Bourns’ products serve essential functions in a rather esoteric fashion. To get us started, Product Line Manager Kurt Wattelet was kind enough to offer a succinct explanation and history of gas discharge tubes as a circuit protection technology. At first, he says, “the old air-gap protector from which the GDT was developed was a very coarse level of protection, easily interjected, ‘though they also tend to be more about precision,’ Wattelet interjects. “Because they also tend to be higher in capacitance with significantly less capability to handle large amounts of current.” To get the same current capabilities of GDTs, large silicon devices are required, and the team at Bourns knew there was a better way.

Very recently, the company has introduced a new GDT series using a breakthrough flat package design. Charting new territory in both volume and space-saving design, the two-electrode Bourns Model 2017 Series FLAT® GDT was, as company representatives point out, put forth specifically to meet “the more sensitive protection requirements of high-density and space-restricted applications in telecommunications and industrial communications equipment, surge protective devices, and printed circuit board (PCB) assemblies.”

According to specs, the new series delivers a rather remarkable 75% reduction in volume as compared to standard 8mm Bourns GDTs.

Johan Schleimann-Jensen, R&D Manager for the FLAT GDT Product Line, adds that the company’s new compact GDT series also offers, “superior surge current ratings, low leakage and insertion loss, and constant capacitance regardless of voltage.” Optimized for long-term reliability and performance, Bourns devices are imbued with voltage limiting capabilities without impacting signal or system operation. To detail, the Model 2017 Series is an ITU K.12 Class III GDT device rated at 10 kA on an 8/20 μs waveform, and features DC breakdown voltages from 90 to 500 volts. The Bourns FLAT GDT also demonstrates an innovative variety of mounting features DC breakdown voltages from 90 to 500 volts. The Bourns FLAT GDT also demonstrates an innovative variety of mounting

According to specs, the new series delivers a rather remarkable 75% reduction in volume as compared to standard 8mm Bourns GDTs.
options, which include bottom-side PCB, horizontal, and vertical surface-mount versions, “as well as a leadless design for cartridge or clamp-fit scenarios.”

Despite the obvious needs that Bourns addresses with the FLAT series, Wattelet makes it clear that a frontier of innovative applications is just opening up for the company’s leading designs. “Another key area is with solar inverters,” he says, highlighting “where companies that design these really small inverters that they place on each solar panel and combine at a central location.” Naturally, he concludes, “size is a big consideration here, and there is clearly a big interest in our reduced footprint.”

Likewise, Wattelet informs us, “The real estate on cell towers is becoming a big issue in the telecommunications world.”

Bourns is now working with companies that, as he describes, “need to cut the circuit board size by half on a particular design, and therefore are looking seriously at the obvious benefits of our FLAT GDT. They are placing them on the top side of a PCB near a connector where you couldn’t normally get a standard GDT.” The company is also working on a three-electrode version of the FLAT GDT, which would essentially combine two tubes into a single device that shares a common, center electrode. Whether saving customers the added steps of modifying many of their products to allow for yesterday’s standard protection measures, or giving the modern infrastructures that define our modern everyday world the reliability that keeps life in motion, Bourns continues an admirable journey to providing the best protection a circuit can get.

The company’s new compact GDT series also offers superior surge current ratings, low leakage and insertion loss, and constant capacitance regardless of voltage.

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We Have a Better Way to Predict PCB MANUFACTURING SUCCESS!

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Having the competitive edge is paramount in today’s PCB manufacturing industry. With outsourcing becoming more and more cost-efficient for prototyping and assembly, American board shops are developing new, unique ways to keep the business in the US and offer significant value at a competitive cost. For Bay Area Circuits, this means overhauling every step of the prototyping process—from design to manufacturing to assembly. EEWeb recently spoke with Stephen Garcia about the primary investments the company has made in equipment, proprietary software, and mechanized assembly—all of which add to the customer-focused approach that makes the outsourcing option obsolete.
Could you give us a little background about yourself and Bay Area Circuits?

My grandfather, Lawrence Nobriga, founded Bay Area Circuits in 1975 so I grew up in and around the business. After college I worked in the technology industry and about 6 years ago returned to take over the leadership of Bay Area Circuits where I’ve tried to apply many of the lessons learned working in a startup environment. Two years ago we relocated to a new facility in Fremont which doubled our capacity. I added a former colleague, Brian Paper, as our COO and Brian and I have worked closely on a variety of marketing, sales and operational efforts in support of our growth plan. This year, we’re proud to be celebrating our 40th year in business.

Bay Area Circuits is a Silicon Valley-based PCB manufacturer that specializes in quick-turn prototypes and small- to mid-sized production runs. Over the last three years, we started to introduce design as well—we have in-house electrical engineer designers. In addition to that, we have added assembly services so that we can offer our customer base the full package, from design to manufacturing to assembly. With ever-shortening deadlines, we have tried to make the process as easy as possible for our customers.

Under my management, we have improved our software design tools and website purchasing experience. We have introduced a suite of free online tools, including downloadable software called PCB Creator that can be used to design a board and place the order directly through the software. More recently, we introduced a tool called InstantDFM, which was the first tool to provide immediate design feedback, meaning a user can upload their design to InstantDFM which will produce a design for manufacturability report and identify any errors that require attention prior to manufacturing. We have really tried to give designers tools to help make them successful.

Our customers represent various industries and geographic markets. Traditionally, a majority of our customer base has been located here in Silicon Valley but today we have a much more national presence. Our demographic also ranges from the student and hobbyist market to professional engineers at the large enterprise level.

The Bay Area is a very expensive region of the country for a company to operate. How does Bay Area Circuits offer competitive pricing given the high cost of operating?

It is definitely a costly region to do business, but it’s also beneficial to be located in the manufacturing hub of Silicon Valley. We focus on technology to try and help lower our costs. We don’t try to compete with offshore manufacturing. Rather, we focus on improving our equipment and making significant investments in the manufacturing process. In the past 18 to 24 months, we have purchased machinery that has really helped increase our capabilities and reduce production cost. It goes even further than equipment though—process and people are key factors to being able to stay competitive and keep our pricing low. To be a manufacturer in North America, we need to utilize today’s available technologies and we have spent as much money on equipment as we have spent on automating the process. I don’t believe there is any company built like us, from the moment we receive a customer’s design data all the way to shipping the order, we have streamlined the process to make it as efficient and cost-competitive as possible.

Do you also offer the opportunity for customers with a 10,000-board run to work with Bay Area in more depth to make sure the order is good to go before going into production?

Yes. Our larger enterprise customers have always represented a significant source of our revenue. A lot of the investment we have made to create tools and processes to assist with the design and purchase process for our online customers are also available to our enterprise customers and help ensure data accuracy prior to production. We also have an internal team of engineers and support staff that utilize the same tools to ensure our customers will receive product that meets their specific requirements. We’re very agile in the way we identify and implement opportunities to strengthen the overall system.
What specific pieces of equipment has Bay Area Circuits invested in over the past year?

Our recent equipment investments have been made with continuous improvement to the manufacturing process in mind which ultimately benefits our customers. Our investments increase our capabilities and quality while ensuring on-time delivery and controlling costs, all of which provides value to our customers. These equipment purchases started last year with the acquisition of an Orbotech Paragon-8000M laser-direct imaging unit. That one piece of machinery really expanded our capabilities and overall quality. At the end of last year, we added an Excellon 136L Intelli-Drill System, which is not only a camera system for inner-layer registration, but doubles as a regular drill with high-speed capabilities. We have to be very lean and flexible as a quick-turn manufacturer, so that piece of machinery has been amazing for us.

When dealing with prototype manufacturing, every minute is important. This year we have added a Seica Rapid 270 Flying Probe Test System, which includes eight probes for high speed testing. But perhaps the acquisition with the potential to make the largest impact has been the Camtek Gryphon, a 3D Functional InkJet Technology system, for the application of solder mask and legend. We were selected to beta test this new technology in a production environment. It is really incredible to see this technology in action; it saves us several hours of process time compared to the traditional process, which is invaluable.

In addition to equipment, we have also worked to broaden the number of services we offer including the addition of new surface finishes to our Plating department which helps reduce production cycle time and increase our overall efficiency and quick turn capabilities.

What do you think is the next game changer for the PCB industry? Will it be in the equipment or requirements?

We have our challenges as a PCB manufacturer in Silicon Valley. I believe the industry should continue to focus on developing new technologies that add value to the manufacturing process. As time goes on, the necessity of equipment has become more important, especially with more complex designs coming into play. We see designers pushing the limits of their designs, and we need to be able to keep up with that demand from our customers. That said, I don’t think there will be one technology or piece of equipment that will change the PCB industry – to stay relevant, I believe you have to understand the needs of your customers and make investments to meet their demands. And for Bay Area Circuits specifically, we will continue to invest in automating the process to remove room for error at every step of the way. I think that is where some companies may be left behind—if you don’t adapt to new requirements, you will be phased out by the global trends.

What makes customers choose Bay Area Circuits versus buying from a competitor?

It would be hard to find a manufacturer that cares as much about the customer as we do. Our investments show how serious we are about this. I believe that most if not all, PCB customers should have a better buying experience from the quote stage all the way to shipping. For someone that purchases anything online, let’s say from a company like Amazon—these companies have set the bar for the online buying experience. For Bay Area Circuits, I want the customer experience to be second-to-none, in line with the high standards of today’s online ordering experience. Whether it is an equipment purchase or a process change, we are always looking at how that change will make this process better for our customers.